In re Patent Application of:
MAZZONI ET AL.
Serial No. **10/088,387**
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In the Claims:

This listing of claims replaces all prior versions and listing of claims in the application.

Claims 1-3 (Cancelled).

4. (Previously presented) A device for sending and receiving digital data that is capable of processing different bit rates from a group of predetermined bit rates, the device comprising:

a channel coding/decoding stage comprising

an interleaver,

a deinterleaver, and

a memory having a minimum size based upon a maximum bit rate of the group of predetermined bit rates and having a first memory space assigned to said interleaver and a second memory space assigned to said deinterleaver, a size of each of the first and second memory spaces being set as a function of the bit rate actually processed by the device.

5. (Previously presented) The device according to Claim 4 wherein said channel coding/decoding stage further comprises a Reed-Solomon coder/decoder connected to said interleaver and said deinterleaver and having a length N.

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6. (Previously presented) The device according to Claim 5 wherein said interleaver provides convolutional interleaving of I branches with $i - 1$ blocks of M bytes, and the deinterleaver provides convolutional deinterleaving with I' branches of $i' - 1$ blocks of M' bytes, I and I' being sub-multiples of N and i and i' being current relative indexes of the branches.

7. (Previously presented) The device according to Claim 6 wherein the size of the first memory space is equal to $I \times (I - 1) \times M/2$ bytes, the size of the second memory space is equal to $I' \times (I' - 1) \times M'/2$ bytes, and the sizes of the first and second memory spaces are set by I, I', M and M'.

8. (Previously presented) The device according to Claim 6 wherein said interleaver and said deinterleaver respectively comprise a first addressing device and a second addressing device, said first and second addressing devices each comprising:

a first counter defining the relative index i or i' of a branch and having a counting limit value;

a second counter defining a number of bytes in a block and incremented each time that said first counter reaches its counting limit value;

a third counter defining the current index of a block
in the branch with index i or i' to be incremented each time the
block in the branch with index i or i' has M or M' bytes; and

an intermediate calculation device for calculating the
address of each branch in said memory from the content of said
first counter.

9. (Previously presented) The device according to Claim
8 wherein said first addressing device further comprises a first
address determination device for determining successive read and
write addresses in said memory of data successively delivered to
said interleaver and said first address determination device, the
successive read and write addresses being determined based upon
values supplied by said intermediate calculation device, said
second and third counters, and the parameter M.

10. (Previously presented) The device according to
Claim 8 wherein said second addressing device further comprises a
second address determination device for determining successive
read and write addresses in said memory of data successively
delivered to said deinterleaver and said second address
determination device, the successive read and write addresses
being determined based upon values supplied by said intermediate
calculation device, said second and third counters, the parameter
M', and the size of the first memory space.

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11. (Previously presented) The device according to Claim 4 wherein said memory comprises a random access memory.

12. (Previously presented) The device according to Claim 4 wherein said memory comprises a dual-port memory.

13. (Previously presented) A device for sending and receiving digital data that is capable of processing different bit rates from a group of predetermined bit rates, the device comprising:

    a channel coding/decoding stage comprising

        and interleaver,

        a deinterleaver,

        a random access memory whose minimum size is fixed as a function of a maximum bit rate of the group of predetermined bits and having a first memory space assigned to said interleaver and a second memory space assigned to said deinterleaver, a size of each of the first and second memory spaces being set as a function of the bit rate actually processed by the device, and

        a Reed-Solomon coder/decoder connected to said interleaver and said deinterleaver and having a length N.

14. (Previously presented) The device according to Claim 13 wherein said interleaver provides convolutional

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interleaving of I branches with $i - 1$ blocks of M bytes, and the deinterleaver provides convolutional deinterleaving with I' branches of $i' - 1$ blocks of M' bytes, I and I' being sub-multiples of N and i and i' being current relative indexes of the branches.

15. (Previously presented) The device according to Claim 14 wherein the size of the first memory space is equal to $I \times (I - 1) \times M/2$ bytes, the size of the second memory space is equal to $I' \times (I' - 1) \times M'/2$ bytes, and the sizes of the first and second memory spaces are set by I, I', M and M'.

16. (Previously presented) The device according to Claim 14 wherein said interleaver and said deinterleaver respectively comprise a first addressing device and a second addressing device, said first and second addressing devices each comprising:

a first counter defining the relative index i or i' of a branch and having a counting limit value;

a second counter defining a number of bytes in a block and incremented each time that said first counter reaches its counting limit value;

a third counter defining the current index of a block in the branch with index i or i' to be incremented each time the block in the branch with index i or i' has M or M' bytes; and

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an intermediate calculation device for calculating the address of each branch in said random access memory from the content of said first counter.

17. (Previously presented) The device according to Claim 16 wherein said first addressing device further comprises a first address determination device for determining successive read and write addresses in said random access memory of data successively delivered to said interleaver and said first address determination device, the successive read and write addresses being determined based upon values supplied by said intermediate calculation device, said second and third counters, and the parameter M.

18. (Previously presented) The device according to Claim 16 wherein said second addressing device further comprises a second address determination device for determining successive read and write addresses in said random access memory of data successively delivered to said deinterleaver and said second address determination device, the successive read and write addresses being determined based upon values supplied by said intermediate calculation device, said second and third counters, the parameter M', and the size of the first memory space.

19. (Previously presented) The device according to
Claim 13 wherein said random access memory comprises a dual-port
memory.

20. (Previously presented) A method for sending and
receiving digital data and processing different bit rates from a
group of predetermined bit rates, the method comprising:

interleaving and deinterleaving the digital data;

setting a minimum size of a memory based upon a maximum
bit rate of the group of predetermined bit rates; and

assigning a first memory space of the memory for
interleaving and a second memory space of the memory for
deinterleaving, a size of each of the first and second memory
spaces being set as a function of the bit rate actually processed
by the device.

21. (Previously presented) The method according to
Claim 20 further comprising performing Reed-Solomon coding and
decoding for a length N of the digital data.

22. (Previously presented) The method according to
Claim 21 wherein interleaving comprises providing convolutional
interleaving of I branches with i - 1 blocks of M bytes, and
deinterleaving comprises providing convolutional deinterleaving
with I' branches of i' - 1 blocks of M' bytes, I and I' being

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sub-multiples of N and i and i' being current relative indexes of the branches.

23. (Previously presented) The method according to Claim 22 wherein the size of the first memory space is equal to I x (I - 1) x M/2 bytes, the size of the second memory space is equal to I' x (I' - 1) x M'/2 bytes, and the sizes of the first and second memory spaces are set by I, I', M and M'.

24. (Previously presented) The method according to Claim 20 wherein the memory comprises a random access memory.